

TECHNICAL SPECIFICATION FOR CHARACTER DISPLAY MODULES

<i>Part No.</i>	08LCD6
	08LCD7
	08LCD8
	08LCD9
	08LCD11

1.0 ABSOLUTE MAXIMUM RATINGS

1.1 For Character Display Modules

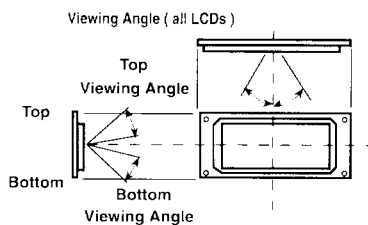
ITEM	SYMBOL	TEST CONDITION	STANDARD VALUE		UNIT
			MIN.	MAX.	
Supply Voltage for Logic	$V_{DD} - V_{SS}$	$T_a = 25^\circ\text{C}$	0	7.0	V
Supply Voltage for LCD	$V_{DD} - V_{SS}$		0	6.5	V
Input Voltage	V_i		V_{SS}	V_{DD}	V
Operating Temperature	T_{opr}	•	0	50	$^\circ\text{C}$
Storage Temperature	T_{stg}	•	-20	70	$^\circ\text{C}$

2.0 OPTICAL CHARACTERISTICS

2.1 For TN Display Modules

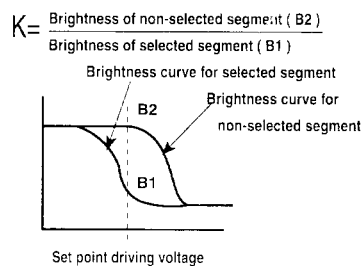
ITEM	SYMBOL	TEST CONDITION	STANDARD VALUE			UNIT	NOTES TO SEE
			MIN.	TYP.	MAX.		
Viewing Angle	θ	$K = 1.4$	10	•	40	degree	1,2
	ϕ		-30	•	30	degree	1,2
Response Time (rise)	T_r	$\alpha = 0^\circ \theta = 0$	•	150	250	ms	3
Response Time (fall)	T_f	$\alpha = 0^\circ \theta = 0$	•	150	250	ms	3

Note 1.) Definition of Viewing Angle

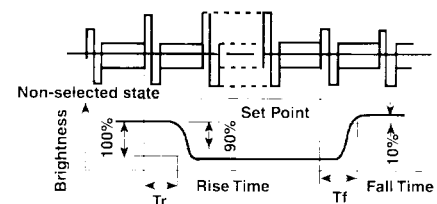


* NOTE: Select either top or bottom viewing angle

Note 2.) Definition of Contrast Ratio "K"



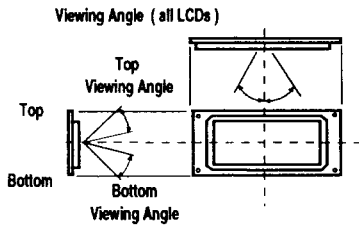
Note 2.) Definition of Optical Response Time



2.2 For STN Display Modules

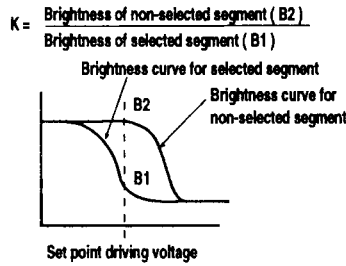
ITEM	SYMBOL	TEST CONDITION	STANDARD VALUE			UNIT	NOTES TO SEE
			MIN.	TYP.	MAX.		
Viewing Angle	θ	$K = 2.0$	-10	•	40	degree	1,2
	ϕ		-30	•	30	degree	1,2
Response Time (rise)	T_r	$\alpha = 0^\circ \theta = 0$	•	250	300	ms	3
Response Time (fall)	T_f	$\alpha = 0^\circ \theta = 0$	•	250	350	ms	3

Note 1.) Definition of Viewing Angle

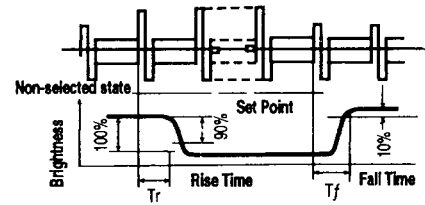


* NOTE : Select either top or bottom viewing angle

Note 2.) Definition of Contrast Ratio "K"



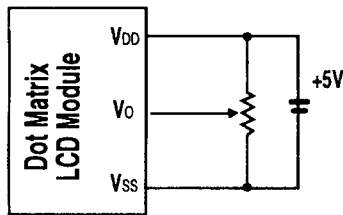
Note 3.) Definition of Optical Response Time



3.0 POWER SUPPLY SCHEMATICS

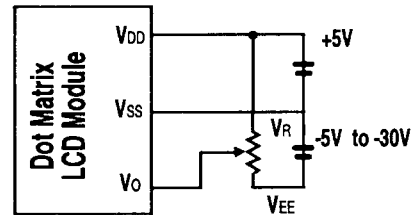
See individual module specification pages for voltage settings to obtain optimum contrast and viewing angle.
NOTE: V_R = Variable Resistor 10 K Ω to 20 K Ω for Adjusting Contrast

3.1 For Single Source



For Modules With Normal Temperature Range Fluid

3.1 For Double Source



For Modules With Extended Temperature Range Fluid or Wide Viewing Cone Fluid

4.0 INTERFACE PIN CONNECTIONS

PIN NO.	SIGNAL	LEVEL	DESCRIPTION	FUNCTIONS
1	VSS	-	Ground	0V
2	VDD	-	Supply voltage for logic & LCD (+)	5v±5%
3	V0	-	Supply voltage for LCD	Decision by user system
4	RS	H/L	Register selection	H : Date L: Instruction code
5	R/W	H/L	Read/Write	H : Read L : Write
6	E	H,H→ L	Enable signal	8 bits
7	DB0	H/L	Data bit 0	
8	DB1	H/L	Data bit 1	
9	DB2	H/L	Data bit 2	
10	DB3	H/L	Data bit 3	
11	DB4	H/L	Data bit 4	
12	DB5	H/L	Data bit 5	
13	DB6	H/L	Data bit 6	
14	DB7	H/L	Data bit 7	

5.0 HOW TO USE LCD CHARACTER MODULE

5.1 Dot Matrix LCD Controller & Driver

The module has a dot matrix LCD controller & driver LSI which is fabricated by low power CMOS technology.

▲ Function

- Character type dot matrix LCD controller & driver.
- International driver : 16 common and 40 segment signal output.
- Display character format : 5x7 dots + cursor, 5x10 dots + 10.
- Easy interface with a 4 - bit MPU.
- Display character pattern : Refer to Standard Character Patterns" 5x7 dots format : 192 kinds, 5x10 dots format : 32 kinds.
- The special character pattern can be programmable by Character Generator RAM directly.
- A customer character pattern can be programmable by mask option.
- Automatic power on reset function.
- It is possible to read both Character Generator and Display Data RAM from MPU.

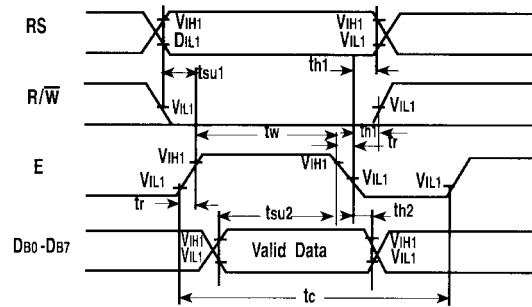
▲ Feature

- Internal Memory
 - * Character Generator ROM : 8320 bits.
 - * Character Generator RAM : 512 bits.
 - * Display Data RAM : 80x8 bits for 80 digits.
- Supply voltage for logic and LCD (+) : +5V±10%.
- Supply voltage for LCD (-) : -5V.
- CMOS process.
- 1/8 duty, 1/11 duty or 1/16 duty : selectable (1/8 duty, 5x7 dots format 1 line, 1/11 duty ; 5x10 dots format 1 line, 1/16 duty : 5x7 dots format 2 lines.)

5.2 Timing Characteristics

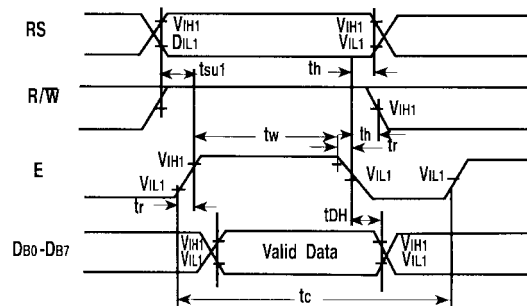
▲ Electrical Characteristics (Ta = 25°C, VDD = 5.0V ± 0.25V, VEE = -19.0V)

CHARACTERISTICS	SYMBOL	STANDARD VALUE			UNIT	APPLICABLE PIN
		MIN.	TYP.	MAX.		
E Cycle Time	tc	500	-	-	ns	E
E Rise Time	tr	-	-	25	ns	E
E Fall Time	tf	-	-	25	ns	E
E Pulse Width (High, Low)	tw	220	-	-	ns	E
R/W and RS Set-up Time	tsu1	40	-	-	ns	R/W,RS
R/W and RS Hold Time	th1	10	-	-	ns	R/W,RS
Data Set-up Time	tsu2	60	-	120	ns	DB0-DB7
Data Hold Time	th2	20	-	-	ns	DB0-DB7



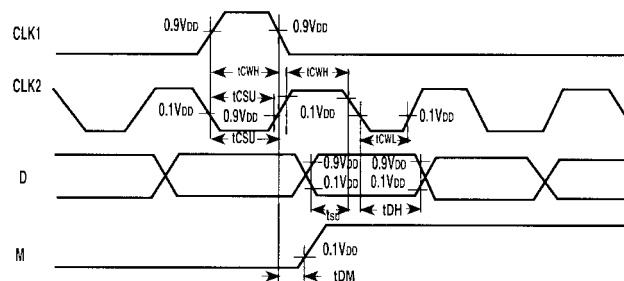
▲ AC Characteristics ($V_{DD}=5V\pm 10\%$, $V_{SS}=25^\circ C$) Write Mode

CHARACTERISTICS	SYMBOL	STANDARD VALUE			UNIT	APPLICABLE PIN
		MIN.	TYP.	MAX.		
E Cycle Time	tc	500	-	-	ns	E
E Rise Time	tr	-	-	25	ns	E
E Fall Time	tf	-	-	25	ns	E
E Pulse Width	tw	220	-	-	ns	E
R/W and RS Set-up Time	tsu	40	-	-	ns	R/W,RS
R/W and RS Hold Time	th	10	-	-	ns	R/W,RS
Data Output Delay Time	tp	60	-	-	ns	DBO-DB7
Data Hold Time	tDH	10	-	-	ns	DBO-DB7



▲ Interface Mode

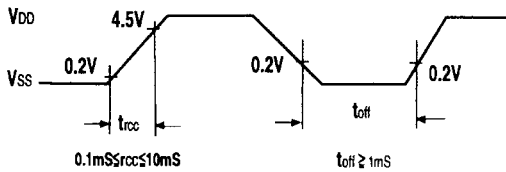
CHARACTERISTICS	SYMBOL	STANDARD VALUE			UNIT	APPLICABLE PIN
		MIN.	TYP.	MAX.		
Clock Pulse Width High	tcWH	800	-	-	ns	CLK
Clock Pulse Width Low	trWL	800	-	-	ns	CLK
Data Set-up Time	tSU	300	-	-	ns	DBO-DB7
Data Hold Time	tDH	300	-	-	ns	DBO-DB7
Clock Set-up Time	tCSU	500	-	-	ns	CLK
M Delay Time	tDM	-1000	-	1000	ns	M



5.3 Power Supply Reset

The internal reset circuit will not operate properly if the following power supply condition is not satisfied. In that case, please perform initial setting according to the instruction.

ITEM	SYMBOL		STANDARD VALUE			UNIT
			MIN.	TYP.	MAX.	
Power Supply Rise Time	trcc	-	0.1	-	10	mS
Power Supply Off Time	toff	-	1	-	-	mS



Note: The item toff defines the time when the power supply shuts down momentarily or repeats on off state.

Reset Function

Initializing by Internal Reset Circuit

The module automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed in initialization. The busy flag (BF) is kept in busy state until initialization ends. (BF=1) The busy state is 10ms after VDD rises to 4.5V.

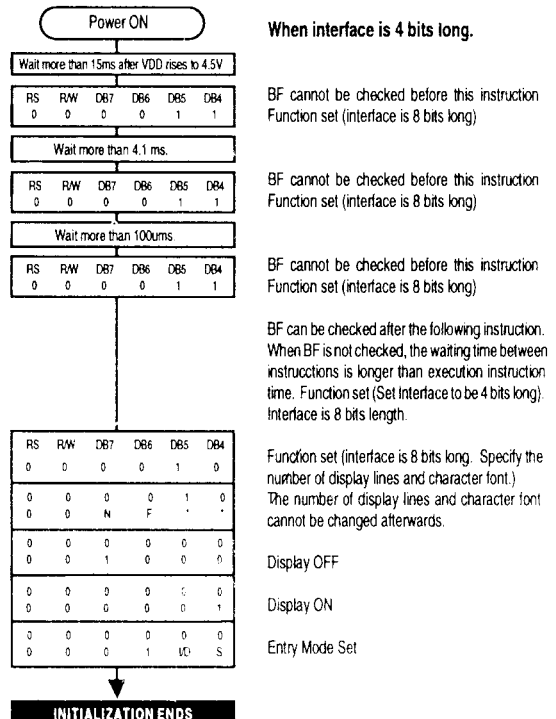
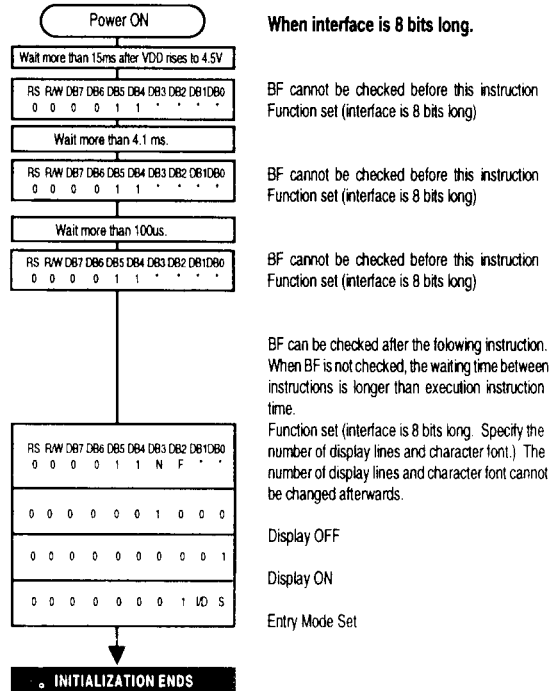
- 1.) Display Clear
- 2.) Function Set
 - DL=1 : 8 bit interface data
 - DL=0 : 4 bit
 - F=0 : 5x7 dot character font
 - N=1 : 1/16 Duty
 - N=0 : 1/8 Duty, 1/11 Duty
- 3.) Display ON/OFF Control
 - D=0 : Display OFF
 - C=0 : Cursor OFF
 - B=0 : Blink OFF
- 4.) Entry Mode Set
 - 1/D=1 : + 1 (increment)
 - S=0 : No shift

Note: When conditions in "Power Supply Conditions Using Internal Reset Circuit" are not met, the internal reset circuit will not operate normally and initialization will not be performed. In this case initialize by MPU according to "Initializing by Instruction".

Initializing by instruction

If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instruction is required.

Use the following procedure for initialization.



5.4 Instructions

INSTRUCTION	CODE										DESCRIPTION	EXECUTE TIME (MAX)	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0).	1.64mS	
Cursor at Home	0	0	0	0	0	0	0	0	1	-	Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DDRAM contents remain unchanged.	1.64mS	
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	40 μ S	
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D) cursor ON/OFF (C), and blink of cursor position character(B).	40 μ S	
Cursor / Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Moves the cursor and shifts the display without changing DDRAM contents.	40 μ S	
Function Set	0	0	0	0	1	DL	N	F	-	-	Sets interface data length (DL) number of display lines (L) and character font (F).	40 μ S	
CGRAM Address Set	0	0	0	1	ACG							Sets the CGRAM address. CGRAM data is sent and received after this setting.	40 μ S
DDRAM Address Set	0	0	1	ADD							Sets the DDRAM address. DDRAM data is sent and received after this setting.	40 μ S	
Busy Flag / Address Read	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	0 μ S	
CGRAM / DDRAM Data Write	1	0	Write Data							Writes data into DDRAM or CGRAM.		40 μ S	
CGRAM / DDRAM Data Read	1	0	Read Data							Reads data from DDRAM or CGRAM.		40 μ S	

CODE	DESCRIPTION	EXECUTE TIME(MAX)
VD = 1 : Increment VD = 0 : Decrement S = 1 : With display shift S/C = 1 : Display Shift S/C = 0 : Cursor movement R/L = 1 : Shift to the right R/L = 0 : Shift to the left D/L = 1 : 8 bit DL = 0 : 4 bit N = 1 : 1/16 Duty N = 0 : 1/8 Duty, 1/11 Duty F = 1 : 5 X 10 dots F = 0 : 5 X 7 dots BF = 1 : Internal Operation is being performed BF = 0 : Instruction acceptable	DDRAM : Display Data RAM CGRAM : Character Generator RAM ACG : CGRAM ADDRESS ADD : DDRAM ADDRESS Corresponds to Cursor Address AC : Address Counter, used for both DDRAM and CGRAM ✖ Invalid	fcp or fosc = 250KHz However, when frequency changes, execution time also changes When fcp or fosc = 270KHz, $40\mu\text{S} \times \frac{250}{270} = 37\mu\text{S}$

● 6.0 DISPLAY CHARACTER POSITION AND CHARACTER

■ 16X1

DISPLAY POSITION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F

DD RAM ADDRESS

■ 16X2

DISPLAY POSITION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

DD RAM ADDRESS

■ 20X2

DISPLAY POSITION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Line 1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
Line 2	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53

DD RAM ADDRESS